TEACHING CHIP SET

The University of Edinburgh and Motorola

General Description

The set comprises four integrated circuits designed for educational purposes:

- CHIP 01: Resistors and Semiconductor Materials
- CHIP 02: MOSFETs
- CHIP 03: Diodes and Photodiodes
- CHIP 04: Ring Oscillator

The chips are in transparent packages allowing the student to view internal structures by microscope. Three of the chips have large scale structures which can easily be viewed by a low power microscope. These structures are resistors, diodes and MOSFETs. The fourth chip has small scale structures requiring a high power microscope for clear resolution.

Each chip has a substrate of n-type doped silicon with a surface area which is 2.5 mm square. Resistors, diodes and MOSFETs have been made by implanting regions of p-type silicon into the substrate. Each chip also has a well of p-type silicon implanted into the substrate. Complementary components have been made by creating n-type implants in the p-wells.

Chips 01, 02 and 03 have sets of similar, matching structures whose lengths, widths, or areas, vary by simple proportion. The dimensions of each structure is specified, permitting values of a wide range of physical quantities to be determined.

Generally all of the components behave in the ideal or normal manner indicated in elementary textbook models. The components are sufficiently large that second order effects are unlikely to be encountered.

Educational significance

Because the aspect ratios of components relate by simple proportion, experiments can be devised to investigate the behaviour of components, or get values of physical quantities. The aspect ratios invite the student to be inquisitive. The dependence of resistance with length or width may be intuitively obvious to many. But here are sets of resistors whose geometrical sizes vary by direct, simple ratios. It calls out for investigating. Perhaps less obvious is what happens to the behaviour of a diode or transistor when one is replaced with another of double the width. Such investigations may push the enquiring student beyond the bounds of electricity or electronics to other areas of physics.

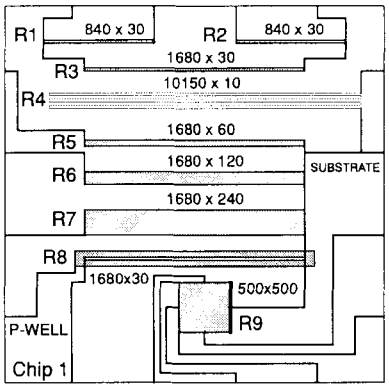
Physical quantities which can be determined include resistivity, conductivity, sheet resistance, mobile charge carrier velocity, mobility and charge carrier density.

The bipolar transistor has gradually been superseded in many applications by the MOSFET. By 1999 more than 90% of transistor structures built on integrated circuits are of a MOSFET type. The prevalence of the MOSFET over other types of structure is expected to continue into the foreseeable future. The four pairs of complementary MOSFETs on Chip 02 allow the student to find out and understand how this device works, and how groups of MOSFETs in complementary pairs form CMOS structures including the inverter, logic gates and memory cells.

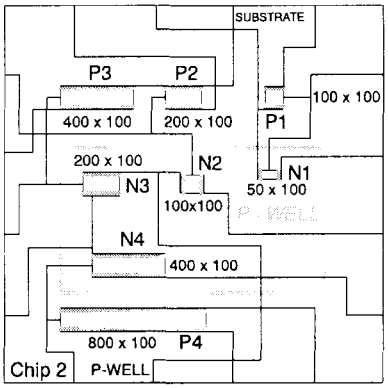
The p-n junction, if exposed to optical radiation, generates electron-hole pairs. In its photovoltaic mode, it acts as a solar cell. In its photoconductive mode, it acts as a light sensor. Both modes of behaviour can be investigated with the photodiodes on Chip 03.

Integrated circuits are almost, always black box devices. The Teaching Chip Set opens a window on this normally obscure subject.

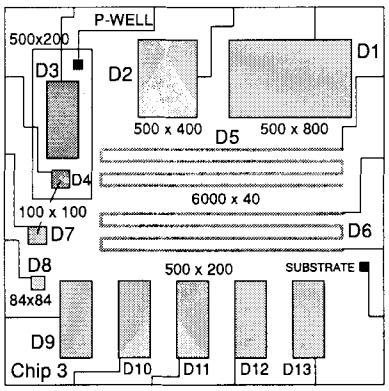
Appearance



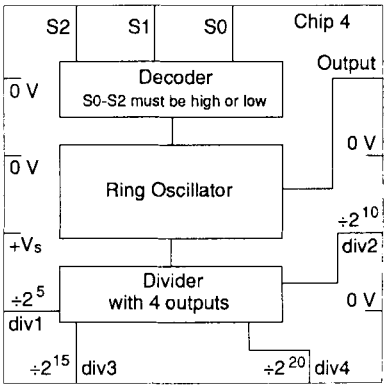
Chip 01: Resistors and Semiconductor Materials



Chip 02: MOSFETs



Chip 02: Diodes and photodiodes



Chip 04: Ring Oscillator

Chip 01
Resistors and Semiconductor Materials

General description

The chip has a substrate of n-type silicon. On top of this are built:

- six p-type heavily doped silicon resistors with different aspect ratios;
- one n-type heavily doped silicon resistor, built on a p-well;
- one metal film resistor (aluminium with a 1% silicon alloy);
- one lightly doped spreading resistor with six peripheral contacts.

It can be used to illustrate series and parallel connection of resistors, show the dependence of resistance on physical size and to derive basic conduction properties of doped silicon and metal films.

Nomenclature

A *plus* sign denotes heavy doping; a *minus* sign denotes light doping. Thus *n* + stands for *heavily doped n-type silicon*; *p* - stands for *lightly doped p-type silicon*. In this context the signs do not refer to electric charge polarity.

Physical properties

Resistor	Material	Length (micron)	Width (micron)	Thick-- ness (micron)	Value (ohm)
R1	p +	840	30	2.4	1130
R2	p +	840	30	2.4	1130
R3	p +	1680	30	2.4	2260
R4	Metal [1]	10150	10	1	30
R5	p +	1680	60	2.4	1130
R6	p +	1680	120	2.4	565
R7	p +	1680	240	2.4	283
R8	n +	1680	30	2.4	870
R9	p -	500	500	7.5	1180 [2]

[1] 99% aluminium, 1% silicon
[2] Measurement between Pin 13 and Pins 9, 10 and 11 commoned

Plan view
Educational applications

Integrated circuit in clear epoxy 16-pin DIL package

- May examine structures with microscope

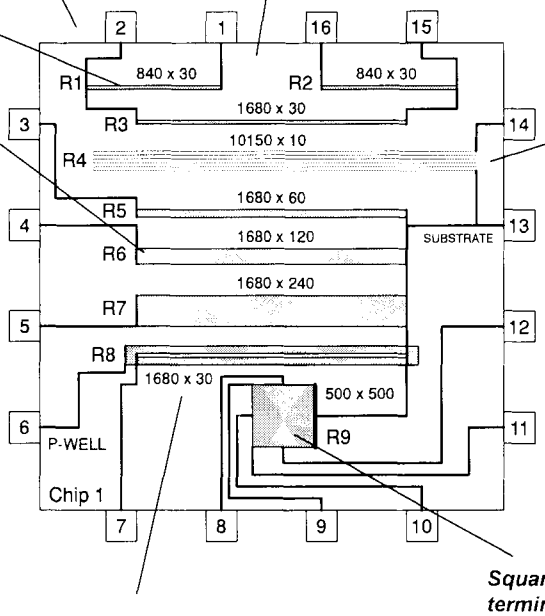
Silicon chip, 2.5 mm square, with n-type silicon substrate

- Seven resistor structures of p-type silicon implanted in substrate
- One n-type silicon resistor implanted in a well of p-type silicon
- One metal film resistor

Resistors of similar cross-sectional area whose lengths vary by 1 : 2

Resistors of similar length and thickness whose widths vary by 1 : 2 : 4 : 8

- Resistors in series and parallel
- Variation of resistance with length and width
- Potential division with matching resistors
- Binary weighted networks
- Electric fields in conductors
- Mobile charge carrier velocity



Aluminium film resistor

- Resistivity comparison between metals and semiconductors
- Temperature dependence of resistance for a metal conductor

Resistors of p-type silicon implanted into n-type substrate

- p-n junction effects
- Photodiodes
- *V - I* characteristics for dark and light conditions

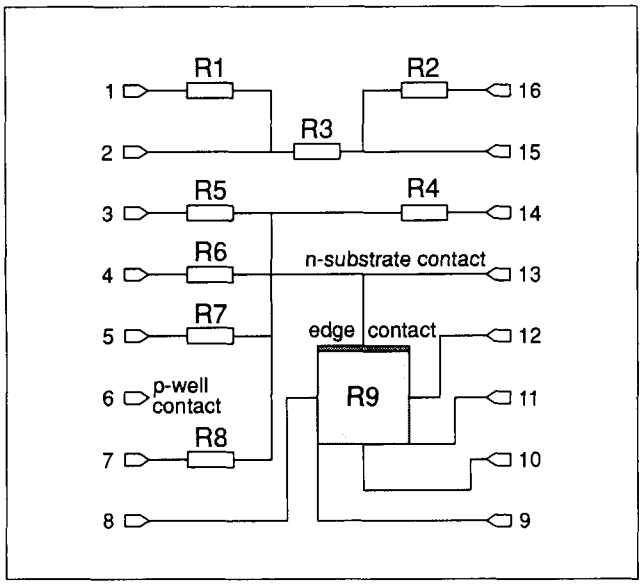
N-type silicon resistor in a well of p-type silicon

- Comparison of electrical properties of n- and p-type silicon

Square resistor of p-type silicon with terminals to sides and corners

- Hall effect
- Determination of sheet resistance, conductivity, hole mobility and charge carrier density
- Modelling with finite element analysis

Circuit diagram

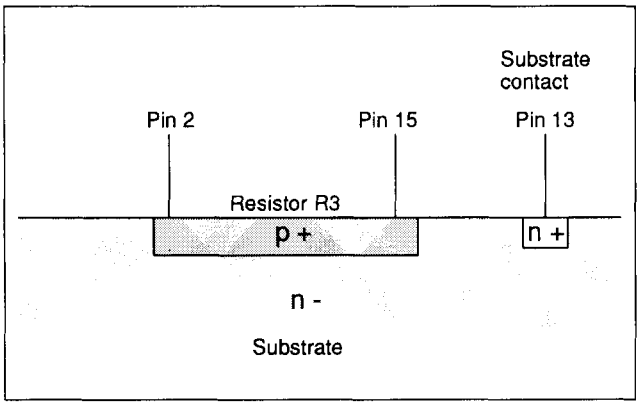


Information on usage

1 The substrate is n-type silicon. Silicon resistors have a parasitic connection to the substrate. Ensure that the p-n junction is always reverse biased.

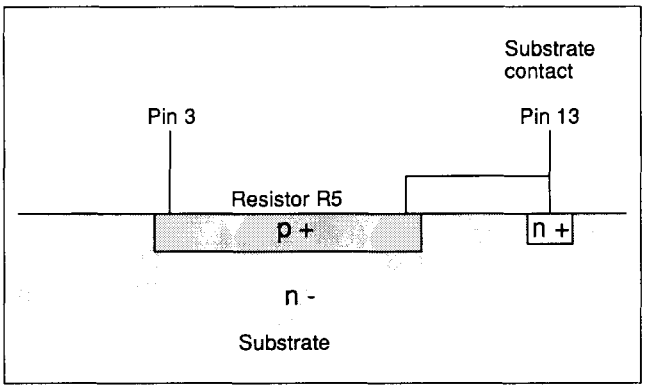
The parasitic p-n junctions are shown in the following set of diagrams. There are three types of structures.

1.1 R1, R2 and R3 are electrically similar. If energized, the polarity of the external supply does not matter provided that other resistors, all of which use pin 13, are not being energized. If pin 13 is being used, it must be at an equipotential or positive potential with respect to other terminals.



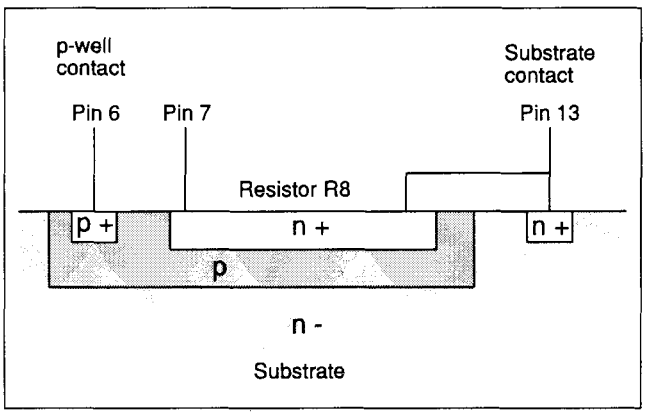
Section through R3 showing external contacts.

1.2 Resistors R5, R6, R7 and R9 are electrically similar. If energized, the polarity of the external supply matters because one terminal of each resistor is electrically bonded to the substrate. Pin 13 must be positive with respect to other terminals.



Section through R5 showing external contacts.

1.3 Resistor R8 is unique. If R8 is unused, pins 6 and 7 may be left floating. If R8 is used, pin 6 must be more negative than either pin 7 and pin 13.



Section through R8.

1.4 The parasitic p-n junctions of R1-3 and R8 may be used as diodes, photodiodes, or photocells. If forward biased, add an external, series resistor to limit the current.

2 The p-n junction between each doped silicon resistor and substrate is light dependent and can behave like a photodiode. Generally the chip should be shielded from light in usage unless its light dependent properties are to be investigated.

3 The absolute maximum power rating of the whole chip is 1 W. The absolute maximum power rating of each resistor is 250 mW. In practice, the power being dissipated should be set much lower than either of these values.

4 If showing the Hall effect with R9, connect pin 13 to the positive terminal of an external supply, common pins 9, 10 and 11 together and connect to the external supply's negative terminal. This establishes a current of holes across R9 from the positive edge contact to the three, negative, point contacts on the opposite side. If a voltmeter is connected across pins 8 and 12, it registers a reading when the chip is placed in a strong magnetic field.

Chip 02
MOSFETs

General description

Chip 02 contains eight, enhancement-mode, MOSFET transistors, of which four are n-channel and four are p-channel. They all have metal gates, using silicon dioxide as the dielectric. The transistors are interconnected to form four complementary pairs from which CMOS structures including the inverter and logic gates may be built.

The p-channel MOSFETs are built directly on the n-channel substrate. The n-channel MOSFETs are built upon a well of p-type silicon implanted in the substrate. The p-well may be regarded as the localised substrate when considering the operation of an n-channel MOSFET.

In order to fit eight MOSFETs on a 16-pin DIL package, none stand as isolated devices, but have interconnections. Transistors may either be used as single components, or in complementary pairs, or in larger groups of transistors as indicated. Some have the substrate internally connected to the source. Where transistors do not have this internal connection, the polarity of the source and drain is set by the experimenter and an external connection is made between the source and substrate.

Physical properties

Transistor	Width (micron)	Length (micron)	Threshold (V)	R_{ON} (kilohm)
N1	50	100	1.8	140
N2	100	100	1.8	70
N3	200	100	1.8	35
N4	400	100	1.8	17
P1	100	100	-1.05	87
P2	200	100	-1.05	43
P3	400	100	-1.05	21
P4	800	100	-1.05	10

Plan view
Educational applications

Integrated circuit in clear epoxy 16-pin DIL package

- May examine structures with microscope
- Metal gate dimensions in microns

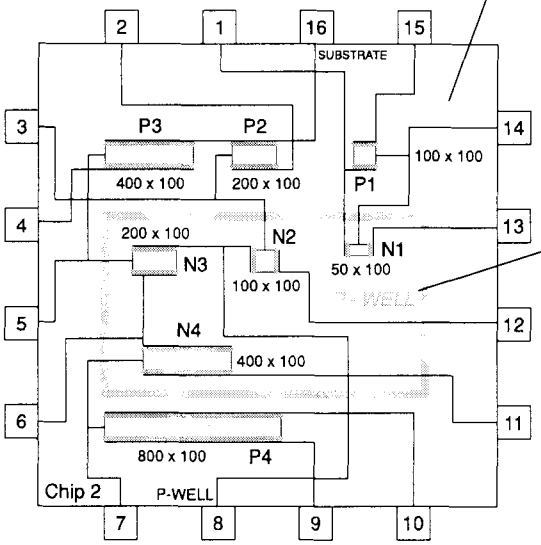
Silicon chip, 2.5 mm square, with n-type silicon substrate

- Four p-channel MOSFETs (P1, P2, P3 and P4) built on substrate
- p-well implanted in substrate

Four complementary pairs of MOSFETs

Applications include:

- CMOS logic devices
- Static and dynamic RAM
- Buffer amplifier
- Ring oscillator
- Voltage to frequency converter
- Analogue switch



Well of p-type doped silicon

- Four n-channel MOSFETs (N1, N2, N3 and N4) built on p-well
- p-well acts as the local substrate for n-channel MOSFETs

Single transistor applications

- Transistor switching
- Constant current source

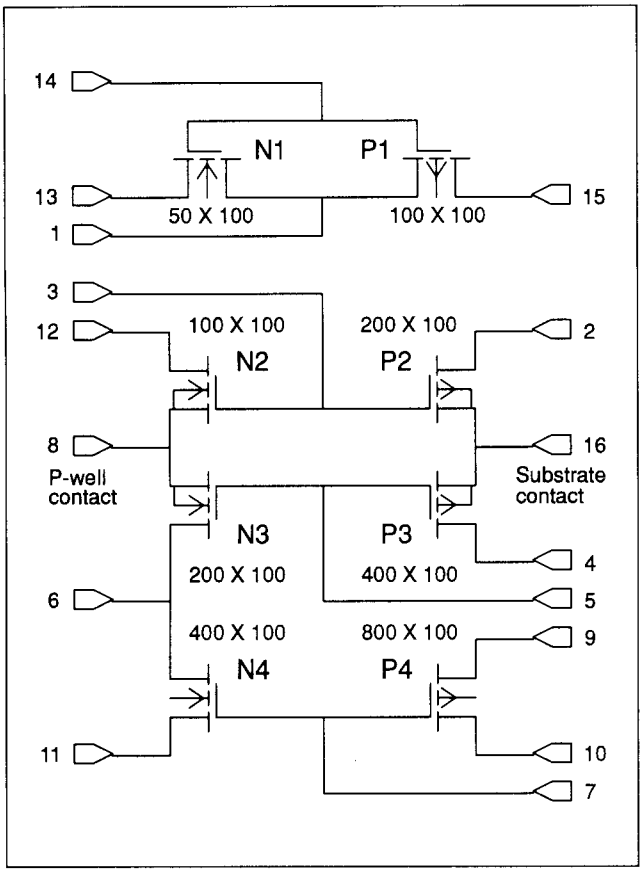
Linear operation investigations

- Drain current versus drain voltage: $I_{DS} = k' V_{DS}$
- Drain current versus gate voltage: $I_{DS} = k''(V_{GS} - V_T)$
- Drain current versus length and width: $I_{DS} = k''' W/L$
- Empirical model: $I_{DS} = k\,(W/L)\,V_{DS}\,(V_{GS} - V_T)$

Non-linear operation investigations

- Drain current versus gate voltage: $I_{DS} = k'(V_{GS} - V_T)^2$
- Drain current versus gate length and width: $I_{DS} = k'' W/L$
- Empirical model: $I_{DS} = k\,(W/L)\,(V_{GS} - V_T)^2$

Circuit diagram



Circuit diagram of Chip 02 showing interconnections of transistors. Gate dimensions are in microns.

Information on usage

1 Interconnections: For eight transistors to fit in a 16-pin DIL package, the transistors are all interconnected. None stands isolated, but any one may be used in isolation as an individual device. When planning to work with two or more transistors, some combinations cannot be made.

Designed complementary pairs are N1 with P1, N2 with P2, N3 with P3, and N4 with P4.

2.1 Supply voltages: Because the p-well forms a p-n junction with the substrate, the junction must be reverse biased. The p-well contact, pin 8, must be connected to the 0 V terminal of an external supply. The substrate contact, pin 16, must be connected to the supply's positive outlet.

Do this even when you are not using transistors connected to these pins.

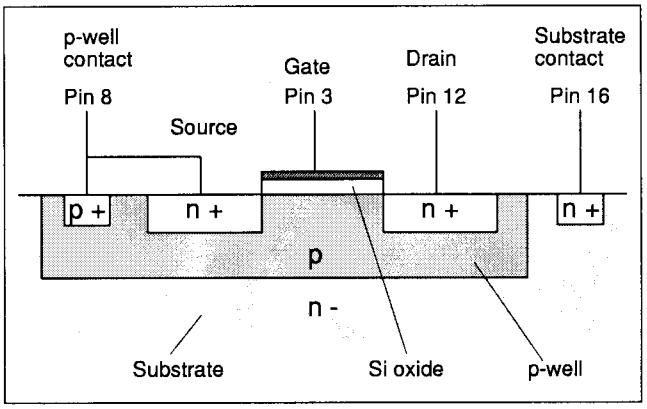
2.2 Never attempt to apply a voltage to any of the transistors at a potential lower than that which you have placed on pin 8. Pin 8 must always be at the minimum voltage of any electrical system.

2.3 Never attempt to apply a voltage to any of the transistors at a potential above that which you have placed on pin 16. Pin 16 must always be at the maximum voltage of any electrical system.

3 Maximum voltage rating: Extreme voltage limits are not known, but would seem to lie in excess of 15 V. We recommend that you do not go above this value.

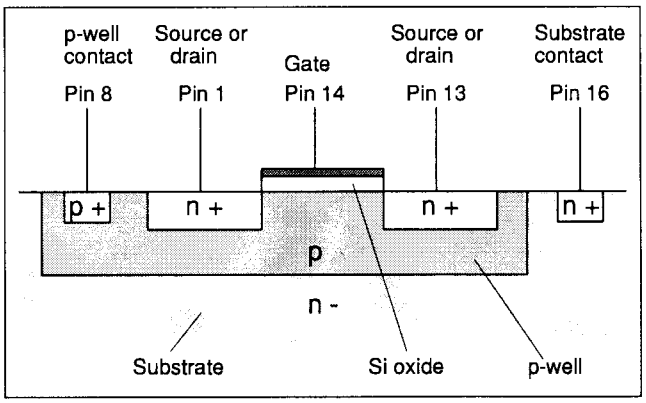
4.1 N-channel devices: The n-channel MOSFETs are built on the p-well. The p-well should be regarded as their localised substrate.

4.2 N2 and N3: Two of the n-channel MOSFETs, N2 and N3, have their sources internally connected to the localised p-type substrate. The p-well contact, pin 8, is the connection to the sources of both N2 and N3. It follows that pin 12 connects to the drain of N2; pin 6 connects to the drain of N3.



Section through N2 showing external contacts. The source is internally connected to the localised p-type substrate. Transistor N3 is similar.

4.3 N1: The source and drain of MOSFET N1 are set by the operator. An external connection must be made between whichever of the pins connecting to N1 is made its source and pin 8, the p-well contact. For instance if you decide to make pin 13 the source of N1, then pins 13 and 8 must be joined by an external, wire connection. Clearly pin 1 would then be the drain.



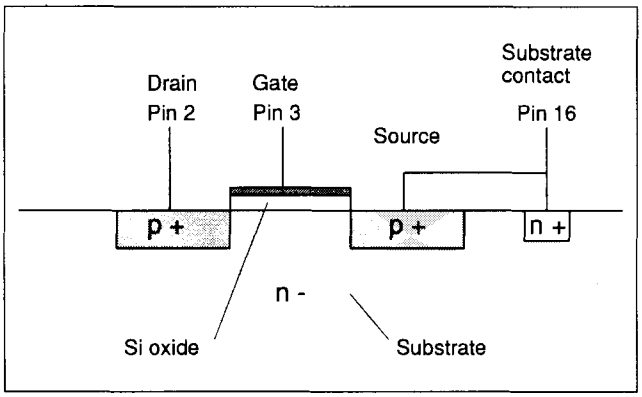
Section through N1 showing external contacts. The operator may set either of pin 1 or pin 13 to be the source.

4.4 N4: Because of the connection from N4 through N3 to pin 8, it is recommended that pin 6 should be the source and pin 11 the drain of N4.

Chip 02
MOSFETs

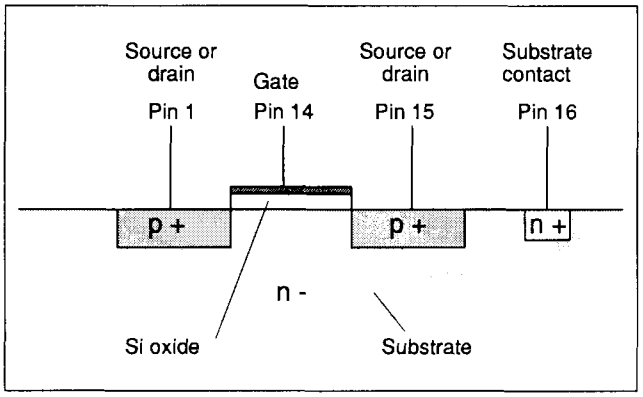
5.1 P-channel devices: The p-channel MOSFETs are built directly on the n-type substrate.

5.2 P2 and P3: Two of the p-channel MOSFETs, P2 and P3, have their sources internally connected to the substrate. The substrate contact, pin 16, is the pin connecting to the sources of both P2 and P3. Pin 2 connects to the drain of P2; pin 4 connects to the drain of P3.



Section through P2 showing external contacts. The source is internally connected to the substrate. Transistor P3 is similar.

5.3 P1 and P4: The source and drain of P1 and P4 are set by the operator. An external connection must be made between whichever pin is made the source and pin 16, the substrate contact. For instance if the implant on transistor P1 connecting with pin 15 is made to be the source, then a connection should be made between pins 15 and 16. In this example if pin 15 connects with the source, then pin 1 connects with the drain.



Section through P1 showing external contacts. The operator may set either of pin 1 or pin 15 to be the source. Transistor P4 is similar.

6.1 Optoelectronic effects: Currents can be generated by light within transistors N4, P2 and P3. (Such currents may be generated whenever light falls on any p-n junction. There are many p-n junctions within the structures on Chip 02.) For some applications it is recommended that the chip should be blacked out.

6.2 The tansistor most greatly affected by light induced currents is N4. This occurs when pin 11 is the source and pin 6 is the drain. A current of nearly 200 microamps may be produced. Ways of avoiding this effect are:

- changing the polarity of N4 by making pin 6 the source and pin 11 the drain (Note 4.4); or
- covering the chip with blackout (Note 6.1); or
- connecting the gate of N3 (pin 5) to 0 V.

6.3 Light induced currents of the order of 20 microamps may affect P2 or P3. It is not possible to prevent these currents by electronic means. The only effective cure is blackout.

7 Unused inputs: Although as a general rule whenever working with MOS devices every unused input should be tied either high or low, this precaution is not needed when using Chip 02. Any transistor, or set of transistors, may be used in isolation. All other transistors can be left floating. However pins 8 and 16 always need to be tied (Note 2.1). If working with N4, pin 5 may have to be tied to 0 V (Note 6.2).

8 Maximum power rating: The maximum power rating of Chip 02 is 1 W.

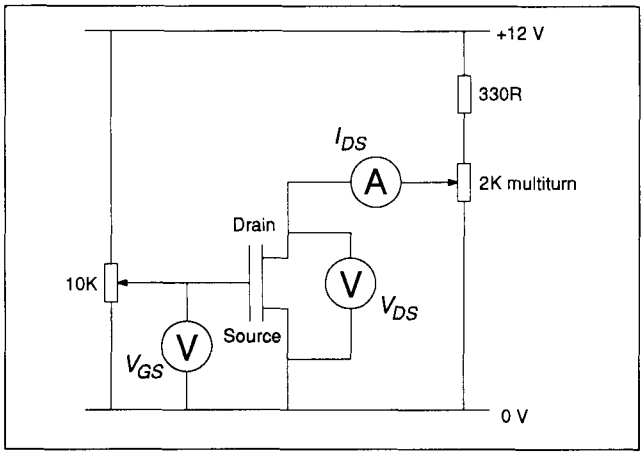
Summary of transistor connections

MOSFET	Gate	Source	Drain
N1	Pin 14	1 and 13 interchangeable	
N2	Pin 3	Pin 8	Pin 12
N3	Pin 5	Pin 8	Pin 6
N4	Pin 7	Pin 6	Pin 11
P1	Pin 14	1 and 15 interchangeable	
P2	Pin 3	Pin 16	Pin 2
P3	Pin 5	Pin 16	Pin 4
P4	Pin 7	9 and 10 interchangeable	

Other specifications

Gate dielectric material ..... Silicon dioxide
Dielectric constant of Si O_2 ..... 3.9
Gate oxide thickness (nm) 100
Source and drain implant depths (micron) 5
Extreme upper operating voltage (V) 15
Recommended upper operating voltage (V) 10
Channel resistance at V_{GS} = 0 V and V_{DS} = 5 V (Gohm) ..... > 10

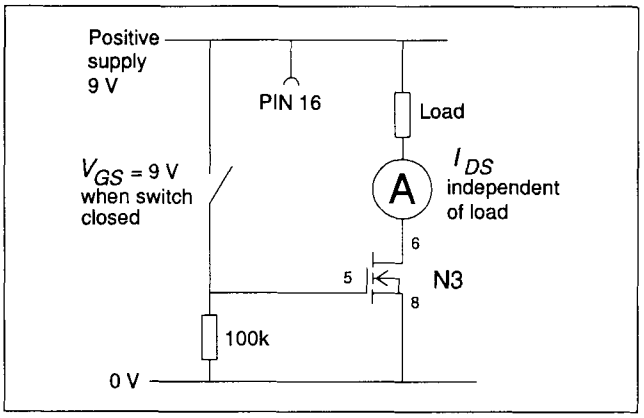
Test circuit



Circuit diagram for experiments on the operating conditions of an n-channel MOSFET.

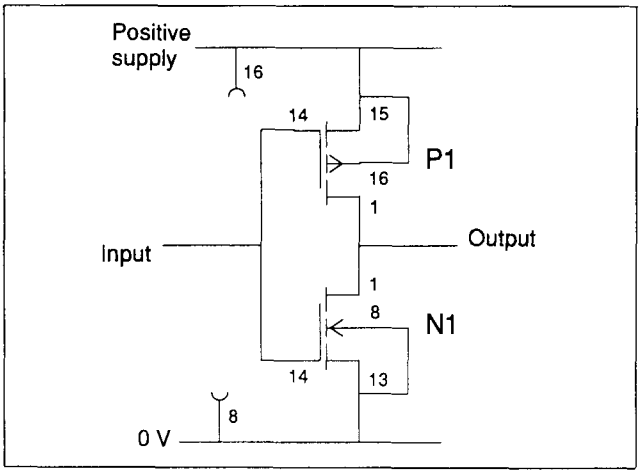
Applications

1 MOSFET switching: At a supply voltage of 9 V, all of the transistors are able to light an LED. The circuit can behave as a constant current source if the load resistance is below a critical value.



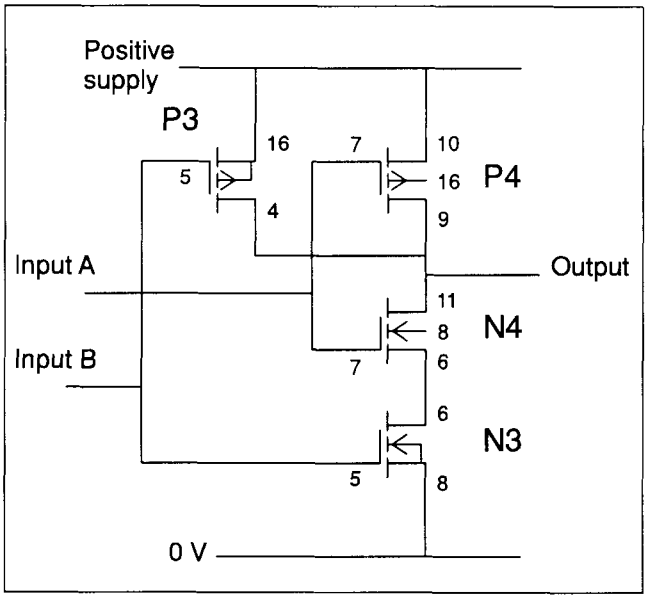
Circuit to show transistor switching.

2 CMOS inverter



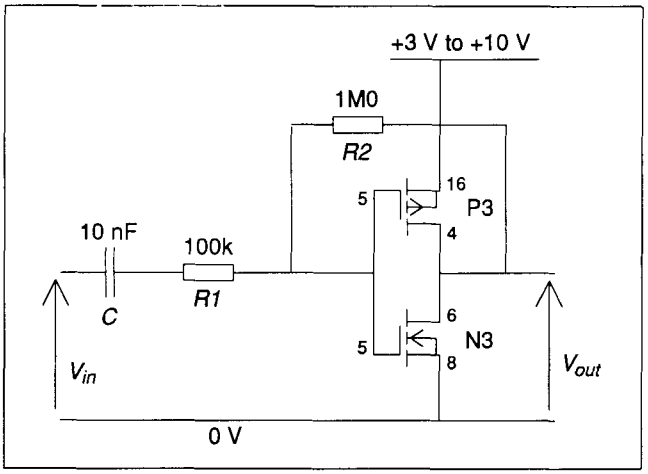
Inverter circuit diagram with complementary pair of transistors, N1 and P1.

3 CMOS 2-input NAND gate



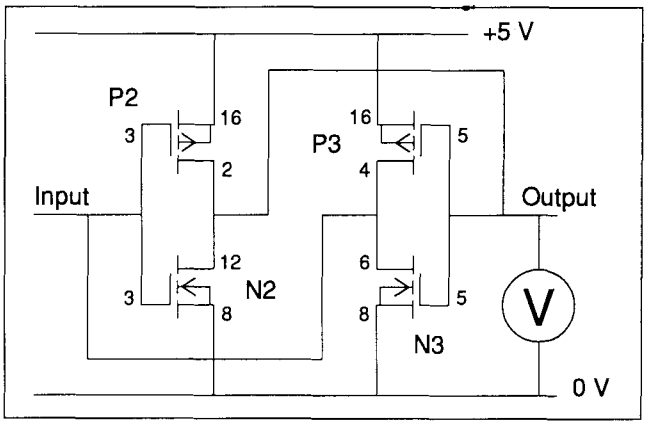
2-input NAND gate circuit diagram.

4 CMOS linear amplifier



Circuit diagram of CMOS linear amplifier.

5 CMOS static RAM



Circuit diagram of CMOS static RAM cell.

Chip 03
Diodes and photodiodes

General description

Chip 02 contains:

- 5 identical p + n photodiodes
- 2 larger area p + n photodiodes
- 2 edge p + n photodiodes
- 1 n + p-well photodiode
- 3 'black' photodiode (devices insensitive to optical radiation)

The p + n diode structures are heavily doped p-type silicon inplanted into the n-type substrate. The n + p-well diodes, of which there are two, one sensitive to light, the other insensitive to light, are implants of heavily doped n-type silicon on a well of p-type silicon that, itself, is implanted in the substrate.

The large area structures can be used to compare the effects of surface area and dopant materials on optoelectronic properties. The array of five photodiodes can be used in optoelectronic switching applications such as detecting the direction or speed of movement, or in diffraction experiments. The edge photodiodes are preferentially sensitive to light at the blue end of the spectrum, whereas the large area photodiodes are more sensitive to red radiation.

Apart from these specialised applications, the diodes and photodiodes may be used to show standard behaviour of a p-n junction and how it is affected by optical radiation. The devices would normally be used as single components, but may be connected in parallel, subject to certain obvious limitations.

Physical properties

Diode	Photo or Black	Doping	Length (micron)	Width (micron)	Max current (mA)
D1	Photo	p + n	800	500	60
D2	Photo	p + n	500	400	40
D3	Photo	n + p	500	200	22
D4	Black	n + p	100	100	17
D5	Photo	p + n	6000	40	35
D6	Photo	p + n	6000	40	7
D7	Black	p + n	100	100	15
D8	Black	p - n	84[1]	84[1]	15
D9	Photo	p + n	500	200	40
D10	Photo	p + n	500	200	40
D11	Photo	p + n	500	200	40
D12	Photo	p + n	500	200	40
D13	Photo	p + n	500	200	40

[1] The junction area of each black diode is 100 micron square. The contact hole of D8 is 84 micron square, but lateral diffusion of the 7 micron deep well takes the junction out to 100 x 100 micron.

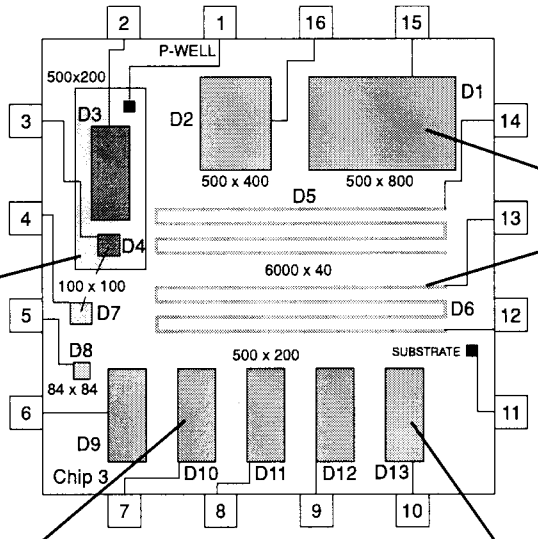
Plan view
Educational applications

Integrated circuit in clear epoxy 16-pin DIL package

- May examine structure by microscope
- Surface dimensions in microns

Silicon chip, 2.5 mm square, with n-type silicon substrate

- Eleven diodes constructed on substrate by implanting areas of p-type silicon. For these diodes the implant is the anode and the substrate is the cathode.
- P-well implanted in substrate
- Two diodes constructed on p-well by implanting areas of n-type silicon. For these diodes the implant is the cathode and the p-well is the anode.



Tests

- Diode and photodiode characteristics
- Dependence of electrical behaviour on surface area and dopant density

Deep junction and edge-effect diodes

- Deep junction diodes are relatively sensitive to red light
- Edge-effect diodes are relatively sensitive to blue light

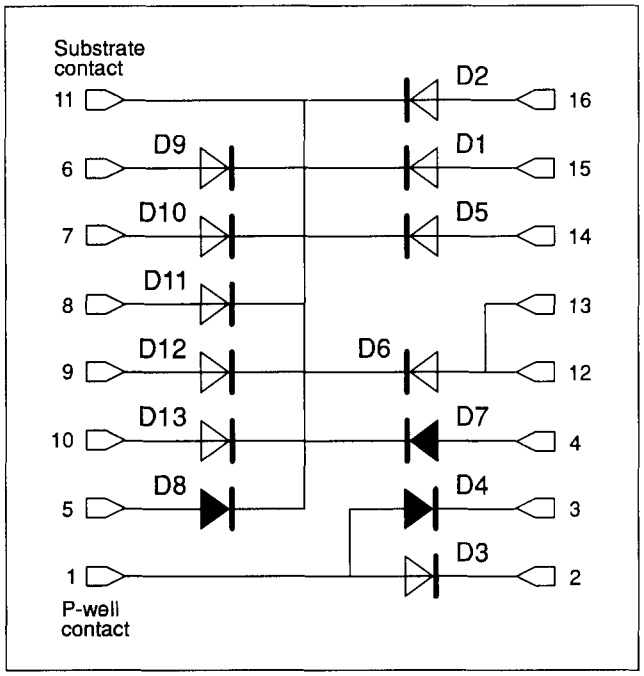
Array of five identical photodiodes

- Direction of movement sensing
- Speed of movement measurement
- Diffraction of light investigations
- Image resolution investigations

Photodiode applications

- Linear light sensor in photoconductive mode
- Miniture detector for the inverse square law
- Solar cell power in photoconductive mode

Circuit diagram



Circuit diagram of Chip 03 showing interconnections of diodes. The blackened symbols represent diodes that are insensitive to light.

Information on usage

1 Interconnections: Generally the diodes are used individually. The eleven diodes built on the substrate have the substrate as a common electrical connection. The substrate is the cathode of these diodes. Any of these diodes may be connected in parallel, but not in series, except if back to back.

The two diodes built on the p-well have their anodes commoned.

2 Current limitation: If forward biasing a diode, add a series resistor of suitable value to keep the current within the tabulated limits (Page 8).

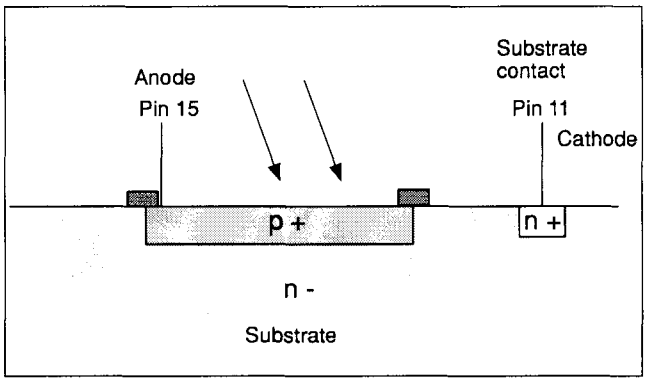
3 Voltage limitation: The maximum forward voltage for all diodes is 0.9 V.

4 p-n junction properties: Three types of diode can be made using the CMOS process. D4, D7 and D8 are examples of the three types. These are all 'black' diodes, so called because the top metal contact covers the whole junction which is thereby shaded from light.

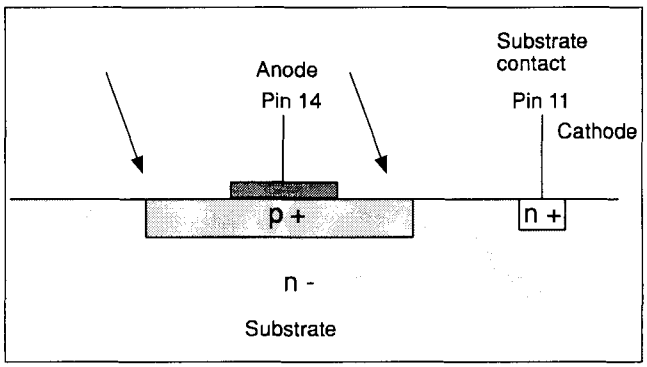
Nine photodiodes have similar p-n junction properties to D7. Photodiode D3 resembles D4.

Black diode	Photo-diode	Layers	Dopant type	Dopant conc. (m^{-3})
D4	D3	Upper Lower	n + p-well	5×10^{26} 10^{22}
D7	D1 D2 D5 D6 D9-13	Upper Lower	p + n-substrate	5×10^{26} 10^{21}
D8		Upper Lower	p-well n-substrate	10^{22} 10^{21}

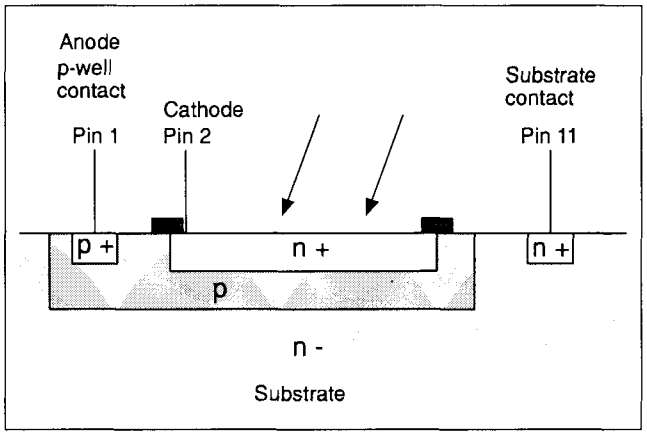
5 Diode sections:



Section through deep junction diode D1. Photodiodes D2 and D9 to D13 are similar. Black diodes D7 and D8 are electrically similar except that the metal contact to the anode covers the entire diode surface. Metal contacts to the photodiodes cover the perimeters.



Section through edge-effect photodiode D5. D6 is similar. The anode contact shades most of the deep-lying part of the p-n junction from light. It is mainly the surface parts that are irradiated. Because silicon absorbs blue light, but transmits red, this type of structure is blue sensitive, whereas the deep-junction diode is red sensitive. The edge length to surface area ratio of D5 and D6 is very large.



Section through photodiode D3. The black diode D4 is electrically similar except that its metallic anode contact entirely covers the surface, shading it from light.

6 Black diodes: Shade from light even although the anodes are covered by metal contacts. Scattered stray light can affect them unless the the entire chip is blacked out.

Chip 04
Ring Oscillator

General description

Chip 04 contains:

- 301-stage ring oscillator
- 3-bit address decoder to configure the chain length
- set of four dividers, each of which reduce the frequency by 2^5
- about 1500 MOS transistors

The transistors in Chip 04 are scaled down versions of the ones found on Chip 02. The respective channel lengths are 9 micron and 100 micron. Even at x 40 magnification, details of Chip 04's transistors are not discernible.

The chip generates oscillations. The frequency is set by the decoder, the divider and the supply voltage. The range extends between 0.02 Hz and 1 MHz.

Educational applications include using the device as a source of oscillations, and investigating how the frequency can be controlled. More fundamentally it reveals the time dependence of any signal being transmitted through an electronic circuit, caused by, in this case, capacitance and resistance. It is also an example of decoding.

Ring oscillator

A ring oscillator has an odd number of CMOS inverters connected in series with the output of the last fed back to be the input of the first. Because of the odd number of stages, the system is unstable and goes into oscillation. The propagation delay in the signal travelling from one inverter to the next inverter is due to the combined effects of gate capacitance and channel resistance.

The output is a square wave where the signal alternates between logic HIGH and logic LOW.

The frequency may be controlled digitally by the 3-bit input applied to the Decoder. The frequency also depends on the supply voltage. As the voltage increases, the charge placed on each transistor gate goes up linearly. However the charging current inceases by the power of two because of the effect of gate voltage on drain current. The net effect is that frequency increases linearly with voltage, subject to an offset for threshold voltages.

A design for a ring oscillator using three complementary MOS transistor pairs from Chip 02 is shown on page 11. The 33 nF capacitors have been added to reduce the frequency, but may be omitted.

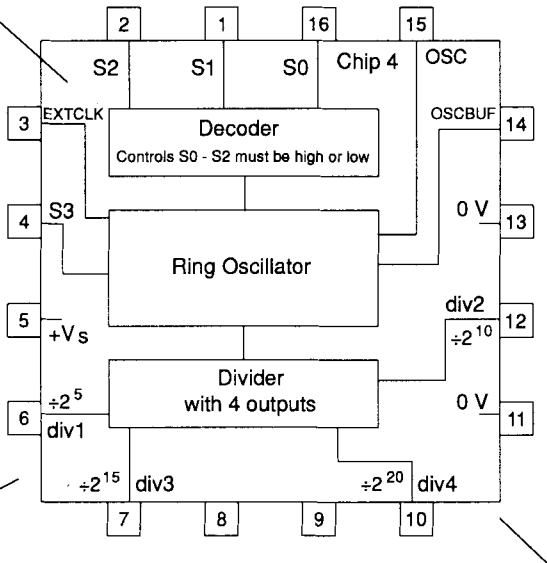
Schematic diagram
Educational applications

Integrated circuit in clear epoxy 16 pin DIL package

- Contains roughly 1500 transistors
- Transistor channel length of 5 micron
- Transistor structures too small to resolve with x 40 magnification

External input facility

- Applies a time delay to digital pulses
- Frequency divider



Ring oscillator with 301 CMOS inverters

- Decoder selects the number of inverters
- The fewer the inverters, the higher the frequency
- Four-stage divider divides the frequency by 2^5, 2^{10}, 2^{15} and 2^{20}
- Frequency range from 0.02 Hz to 1 MHz

Educational significance

- Example of time delays in digital logic caused by combination of capacitative and resistive effects

Investigations include:

- Frequency dependence on a decoder controlled by 3-bit logic
- Frequency division and powers of two
- Frequency dependence on supply voltage

Applications include:

- Source of oscillations for other projects
- Voltage to frequency conversion
- Music synthesizer when controlled by a programmable logic device

Chip 04
Ring Oscillator

Function	Label	Pin	Notes
Decoder	S2 S1 S0	2 1 16	High bit Low bit See separate table
Selector	S3	4	L = Ring oscillator H = Inverter chain
Outputs	OSC OSCBUF	15 14	Unbuffered output Buffered output
Divider	DIV 1 DIV 2 DIV 3 DIV 4	6 12 7 10	Divide by 2^5 Divide by 2^{10} Divide by 2^{15} Divide by 2^{20}
Input	EXTCLK	3	Signal input to inverter chain if S3 = HIGH Tie EXTCLK to 0 V if S3 = LOW
Supply	$+V_S$ 0 V 0 V	5 11 13	Positive supply 0 V potential 0 V potential
		8 9	No connection No connection

Chip 04 pin specifications.

S2	S1	S0	Inverters in ring
0	0	0	21
0	0	1	31
0	1	0	61
0	1	1	91
1	0	0	121
1	0	1	181
1	1	0	241
1	1	1	301

Input states of decoder.

S3	Function
0	Ring oscillator selected
1	External pulses from EXTCLK

Input states of External Clock Selector S3.

Information on usage

1 Pins 11 and 13 must always be connected to 0 V.

2 Pin 5 must be connected to the positive supply before, or at the same time as, connecting a signal to any other input.

3 The supply voltage may be varied between about 2.5 V and 10 V. The oscillation frequency increases linearly with the supply voltage.

4 The value of an input signal voltage must not exceed the supply voltage value. Generally input signals would be at the same potential as the supply.

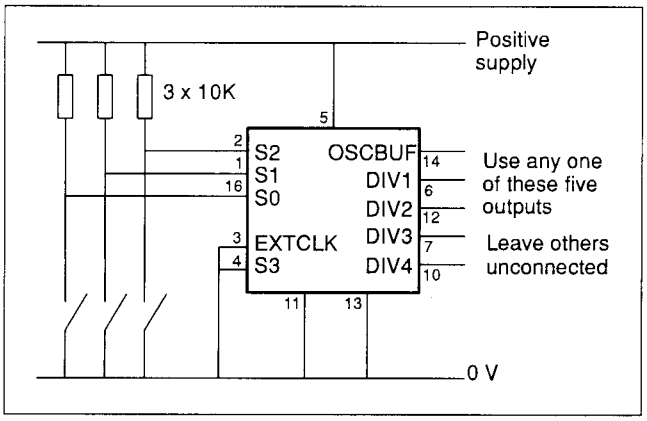
5 Unused inputs should be connected to 0 V. This rule applies to both of EXTCLK and S3 when Chip 04 is being used as a ring oscillator. Some, or all of, S0, S1 and S2 may also have to be tied to 0 V.

6 Unused outputs should be left floating. This applies to them all (OSC, OSCBUF, DIV 1, DIV 2, DIV 3 and DIV 4).

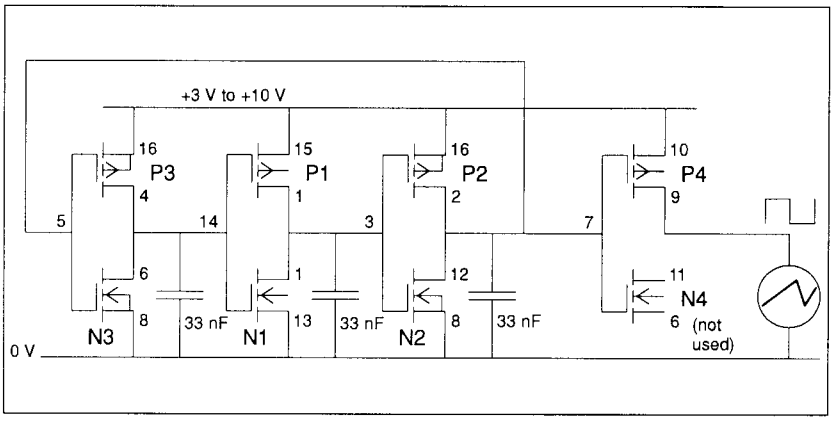
7 Preferentially use the buffered output OSCBUF, or any of the Divider outputs, for examining oscillations on a CRO, of for measuring frequency. Do not use the unbuffered output OSC because the impedance of a load placed on OSC affects the period of oscillation.

8 If the load placed on either the buffered output OSCBUF, or any Divider output, is too great such that a significant current is drawn, then the oscillation frequency will reduce. This is because a large output current pulls down the working voltage to the ring oscillator's transistors. This causes a reduction in frequency. For example if an output were to be loaded with an LED, then frequency would fall. This difficulty can be got round by using an external transistor to drive the LED.

Applications



Chip 04 wired as a ring oscillator.

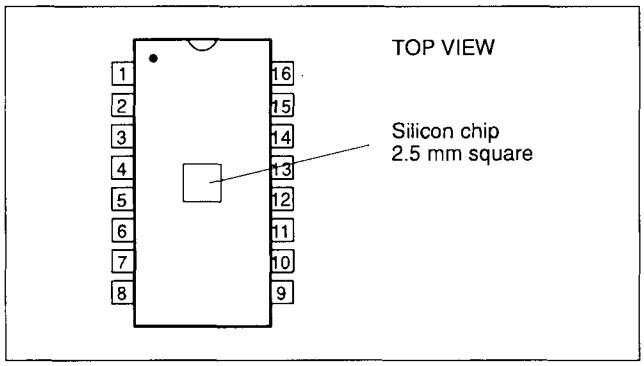


Ring oscillator using transistors on Chip 02. P4 buffers the output. The capacitors lower the frequency and may be omitted.

TEACHING CHIP SET

The University of Edinburgh and Motorola

Plan of DIL package



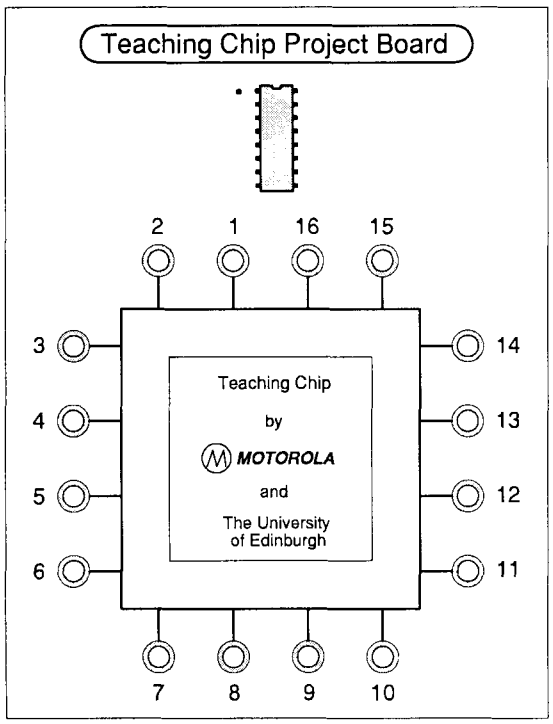
Practical usage

1 Prototype board.

2 Boards with a 16-pin DIL socket with connections to 4 mm socket outlets made by JJM Electronics:

Teaching Chip Project Board, for use with any of the Chip Set (illustrated below) *£13.25*
Resistance and Length, for use with Chip 01 ..... *£6.50*
Resistance and Width, for use with Chip 01 ..... *£6.75*
Ring Oscillator, for use with Chip 04 ..... *£11.75*

JJM Electronics
Meft Road
Urquhart
Moray IV30 8GG



JJM Teaching Chip Project Board

Ordering details

Set of 4 Teaching Chips (01, 02, 03 and 04) *£6.00*
Any single chip (01, 02, 03, or 04) *£2.00*

Chips supplied by SSERC

Publications

Standard Grade Physics Practical Investigations (set of 8 investigations): Teaching Chip Project.
Optoelectronics and Semiconductors in Higher Physics (set of 7 experiments): Teaching Chip Project.
Practical work with Chip 01: SSERC.
Modelling resistor behaviour with finite element analysis: SSERC.
MOSFETs: Guidance for teachers of Higher Physics (operational description, set of 10 experiments): SSERC.
MOSFETs: Empirical and mathematical modelling: SSERC.
Light intensity experiments with Chip 03: SSERC.

Publications supplied by SSERC. Price on application.

Further information

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Web site: www.sserc.org.uk

Edinburgh University web site:
www.ee.ed.ac.uk/profiles/research/STR/emf/tchip.html

Teaching Chip Project

The Teaching Chip Set was devised and designed in the early 1990s by a team within the Department of Electronics and Electrical Engineering led by Professor John Robertson. The original educational materials including datasheets were written by Peter Bates, at that time a physics teacher seconded to work in the Department. The chip masks were prepared by Compugraphics. The chips were made at the metal gate fabrication facility of Motorola at East Kilbride. Project sponsors were Motorola, Compugraphics, Scottish Enterprise and Lothian Regional Council.

This data sheet has been written by staff at SSERC (December 1999).